WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising an array of rows and columns of memory cells each disposed at an intersection between a digit line and a word line, wherein said array of rows and columns of memory cells is subdivided into a plurality of substantially equivalent partial arrays of rows and columns of memory cells, said plurality of partial arrays arranged with respect to one another such that at least first and second elongate intermediate areas are defined between said adjacent pairs of said plurality of partial arrays, and said partial arrays being further subdivided into a plurality of sub-arrays, said memory device further comprising:

row address predecoding circuitry, disposed in said first intermediate area between a pair of said partial arrays, responsive to row address signals supplied to said device to generate a plurality of predecoded row address signals; and

a plurality of local row address decoding circuits, each associated with and disposed proximally with respect to one of said sub arrays and each electrically coupled to said row address predecoding circuitry to receive said predecoded row address signals, said local row decoding circuits selectively responsive to said predecoded row address signals to apply at least one word line driving signal to its associated subarray during a memory access cycle.

2. A memory device in accordance with claim 1, further comprising:

column address decoding circuitry, disposed in said first intermediate area, said column address decoding circuitry selectively responsive to column address signals applied to said device to apply at least one column select to a plurality of said sub-arrays in at least one of said partial array blocks.

3. A memory device in accordance with claim 2, further comprising:

a plurality of primary input/output lines, extending along said first intermediate area;

a plurality of secondary input/output lines, each selectively coupled to a plurality of said sub-arrays and selectively coupled to at least one of said plurality of primary input output lines.

4. A memory device in accordance with claim 3, further comprising:

a plurality of primary sense amplifiers, each primary sense amplifier disposed adjacent to at least one sub-array and responsive to application of a column select signal to said sub-array to sense a voltage differential on said digit lines in said array.

5. A memory device in accordance with claim 4, further comprising:

a plurality of secondary sense amplifiers, each disposed in said first intermediate area and selectively coupled to said primary sense amplifiers via said secondary input/output lines.

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